## REMARKS

This Request for Reconsideration is submitted in response to the non-final Office Action of July 17, 2006 (hereinafter "the Office Action"). Claims 1-3, and 20-25 remain pending.

All references to the claims, except as noted, will be made with reference to the claim list above beginning on page 2. Unless the source document contains line numbers (e.g., issued U.S. patents) all citations herein containing line numbers will count every printed line, except the page header, but including section headings. If there is any confusion or questions regarding any aspect of this Amendment, the Examiner is invited to contact the undersigned.

***Status of claims***

Claims 1-3 and 20-27 stand rejected under 35 U.S.C. § 103(a) based on newly-cited art. Applicants note with appreciation the withdrawal of previous objections and rejections under 35 U.S.C. § 103 and the issuance of the non-final Office Action of July 17, 2006, so that Applicant has an opportunity to address the new reference.

***Amendment***

This Request for Reconsideration contains no amendments.

***Claim Rejections - 35 U.S.C. § 103(a)***

Claims 1-3 and 22-23 stand rejected under 35 U.S.C. § 103(a) for being unpatentable over U.S. Patent 5,375,216 issued to Moyer et al., hereinafter referred to as "Moyer," in view of U.S. Patent 5,562,380 issued to Brodnax et al, hereinafter referred to as "Brodnax." Applicants respectfully traverse because each and every limitation is not taught or suggested by the prior art, and because the prior art lacks adequate teach, suggestion, or motivation to combine and/or modify the references as proposed in the Office Action.

Claims 1 and 22 set forth, inter alia, that "the backing register file . . . in at least one mode, is always visible outside the processor and is directly accessible to instructions in the programs at any privilege level" (lines 9-12 of claim 1 and lines 4-6 of claim 22). The Office Action suggests that Brodnax teaches this feature at col. 3, lines 21-51, Figure 2, and Figure 3 (Office Action, page 3, line 20). Specifically, the Office Action identifies the shadow register file of Brodnax being a backing register file, and that the shadow register file is directly accessible to instructions (Office Action, paragraph bridging pages 3 and 4).

Applicant initially notes that claims 1 and 22 both provide that the backing register file . . . in at least one mode, is . . . directly accessible to ***instructions in the programs at any privilege level***." The ***programs*** are the ones that execute on the execution unit coupled to the at least one register file (claim 1, lines 3-4) and for which the at least one register file is available for temporarily storing operands and results (claim 1, lines 3-4). The Office Action only mentions that the shadow register is "accessible to instructions" and points to the data cache unit of Moyer as being "accessible" via the load/store unit (Office Action, page 3, lines 17-18). Apparently, the Office Action cites the data cache of Moyer for providing "accessibility" to the program instructions, and shadow register of Brodnax for "directly accessible to instructions." However, the only possible "instructions" which have access to the shadow register of Brodnax is fixed point processor (FXP) microcode (col. 3, lines 60-62). Thus, the feature of providing ***direct*** access to the backing register file by ***instructions in the programs at any privilege level*** mentioned in the claims is not met by either reference individually ***or*** in combination.

Brodnax is directed to a shadow register file for the purpose of maintaining a state of the general purpose registers (GPR) at a "checkpoint" by copying the contents of the GPR to the shadow register file. A checkpoint is established when a memory write is executed (col. 3, lines 16-20). If an error occurs, the processor state is rolled back to the checkpoint by copying the contents of the shadow register back to the GPR (col. 3, lines 18-20). This operation is performed automatically and transparently to the programs (col. 3, lines 65-67). There is no mention in Brodnax that the shadow register file is directly accessible to "the programs executing in the instruction unit that is coupled to the register file." Furthermore, there is no suggestion that the microcode which reads each of the shadow register locations and transfers the contents to the putaway bus (Brodnax, col. 3, lines 60-62) executes on an execution unit that is coupled to the at least one register file. Even if it did, the microcode cannot execute on "the execution unit" as claimed since the claims specify that the backing register file is inaccessible to the execution unit (claim 1, lines 9-10; claim 22 line 4), and the shadow register of Brodnax is accessible to the "microcode" executing in the fixed point processor (FXP 18). Furthermore, the microcode does not read on "the programs" because Brodnax does not suggest that the at least one register file is available to the microcode for temporarily storing operands and results, the only function of the microcode being to move data from the shadow register to the putaway bus.

Since the independent claims 1 and 22 provide that "the backing register file . . . in at least one mode, is always visible outside the processor and is directly accessible to instructions in the programs at any privilege level" and neither Brodnax nor Moyer teach or suggest this feature, Applicants respectfully submit that claims 1 and 22 are allowable over the cited prior art of record.

With regard to claims 2 and 23, neither Brodnax nor Moyer teach or suggest "allowing transfer of values from any designated location in any designated register file of said plurality of register files to any designated location in said backing register file, and from any designated location in said backing register file to any designated location in any register file of said plurality of register files" (claim 2, lines 5-8; claim 22, lines 3-7). The data cache of Moyer are not registers, therefore the program cannot assign a particular value to a particular location in the cache. Depending on the associativity of the cache, which is not specified by Moyer, the value may depend on the physical address of the location it is stored in main memory, or it may store a value based on a least-recently-used algorithm, and therefore be completely out of the control of the software as to where the value is stored in the cache. Because the cache stores a copy of a small subset of the main memory, each storage location in the cache can correspond to numerous possible storage locations in the main memory and therefore has no assigned address. Likewise, the shadow register of Brodnax only permits wholesale copying of the general purpose registers to the shadow registers. As shown in Figure 2, each general purpose register 22, 24, 26, has a single corresponding shadow register 22', 24', 26' to which data may be copied. Thus, Brodnax is also incapable of "allowing transfer of values from any designated location in any designated register file . . . to any designated location in said backing register file" as set forth in lines 3-5 of claims 2and 23.

The Office Action cites Moyer column 6, lines 50-64; Figure 1; Figure 5; Figure 6; and Figure 7 as reading on this feature (Office Action, page 4, lines 10-19). Applicants have carefully reviewed the indicated portions of Moyer but do not see any suggestion of moving data from any designated location in any designated register file of Moyer to any designated location of the data cache. As mentioned above, the data cache is not addressable memory and therefore does not support placing a value in a designated location. The addresses mentioned by Moyer are either "effective addresses" which is Moyer's terminology for virtual addresses, or physical addresses, and these do not specify a location in the cache, but a location in main memory. Depending on the associativity of the cache, the possible locations

are either restricted depending on the location of the data in the main memory, or out of the control of the software.

For the above-stated reasons, neither of Brodnax and Moyer teach or suggest "allowing transfer of values from any designated location in any designated register file of said plurality of register files to any designated location in said backing register file, and from any designated location in said backing register file to any designated location in any register file of said plurality of register files" as set forth in claim 22. Therefore, claims 2 and 23 should be allowed over Brodnax and Moyer.

With regard to claims 26 and 27, the Office Action suggests that "as taught by InstantWeb [a person having ordinary skill] would have recognized that a register faster and typically can read two (sic) register and write to a register all in a single cycle . . . thereby increasing speed of the processor. Therefore, it would have been obvious . . . to incorporate the registers of InstantWeb in the device of Moyer to increase processor speed" (Office action, pages 6-7). By these statements, it appears that the Examiner is suggesting that it would be obvious to provide each of the plurality of memory locations in the data cache (which the Office Action notes is a "backing register file" --- see Office Action, page 3, lines 13-14) with the ability to be accessed at random using a uniquely assigned address as set forth in claims 26-27. Applicant respectfully disagrees. Yes, InstantWeb teaches a register file having addresses that allow fast access. However, there is no suggestion, teaching, or motivation in InstantWeb or elsewhere in the prior art to provide a data cache, such as that taught by Moyer, with the ability to access at random each memory location therein by assigning each memory location with a unique address. Therefore Neither Moyer nor InstantWeb, or any other reference of record teaches or suggests a backing register as claimed in claims 26 and 27.

Claims 20, 21, 24, and 25, stand rejected under 35 U.S.C. § 103(a) for being unpatentable over Moyer, Brodnax, and Wikipedia. These claims are directed to using the backing register to mimic register windowing functionality (e.g., claim 20, lines 2-3). The Examiner suggests that, since register windowing was known as evidenced by Wikipedia, it would have been obvious to use the data cache of Moyer in the same manner. Applicants respectfully disagree. There is no suggestion in the prior art that it even would be ***possible*** to use a data cache to mimic register windowing. Data caches, such as that taught by Moyer, are not addressable, and therefore cannot function in a register windowing mode; by their very nature, windowing registers must be addressable.

The prior art lacks any teaching, suggestion, motivation to combine and/or modify the references as proposed in the Office Action. The Office Action suggests that "it would have been obvious . . . to incorporate the shadow registers of Brodnax in the device of Moyer to improve fault tolerance and error correction" (Office Action, page 4, lines 3-6). Applicant agrees that it ***may*** have been obvious to incorporate a shadow register of Brodnax into the device of Moyer. However, the Office Action goes ***far beyond*** simply incorporating a shadow register into the device of Moyer, which would result in a system including both a data cache (as taught by Moyer) and a shadow register (as taught by Brodnax). However, the combination cobbled together in the Office Action includes features that lack any motivation. For example, the Office Action provides that the combined device will be always visible outside the processor as described in Moyer, which teaches instructions that manipulate cache control (Office Action, page 3, lines 1-16). If the motivation is "to improve fault tolerance and error correction" as asserted in the Office Action (page 4, lines 5-6) then there is no need for it to be visible to programs since making it available and visible to programs does nothing to improve fault tolerance and error correction. Thus, there is no correlation between the motivation to combine, and the combination proposed. That is to say, the motivation suggests one combination, but to meet the claims, the Office Action combined the references in a different way. The actual combination proposed is not suggested by the prior art, and the motivation to combine can only have come from Applicants' own disclosure. Therefore, Applicants respectfully submit that the combination proposed constitutes impermissible hindsight under 35 U.S.C. § 103(a).

Since there was no motivation to modify the prior art references as proposed in the Office Action, and because there was no reasonable expectation of success to make the combination as proposed, Applicants respectfully submit that the claims are patentable under 35 U.S.C. § 103(a).

For the reasons listed above, Applicants respectfully submit that this application is now in condition for allowance and earnestly request the same. Should any issue remain outstanding, Applicants invite the Examiner to contact the undersigned so that any remaining issues can be quickly resolved. Likewise, if the Examiner has any questions or concerns regarding the present Amendment, the Examiner is invited to contact the undersigned at (408) 774-6933.

If any fees are due in connection with filing this amendment, the Commissioner is also authorized to charge Deposit Account No. 50-0805 (Order No. SUNMP298). A duplicate copy of the transmittal is enclosed for this purpose.

Respectfully submitted,
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